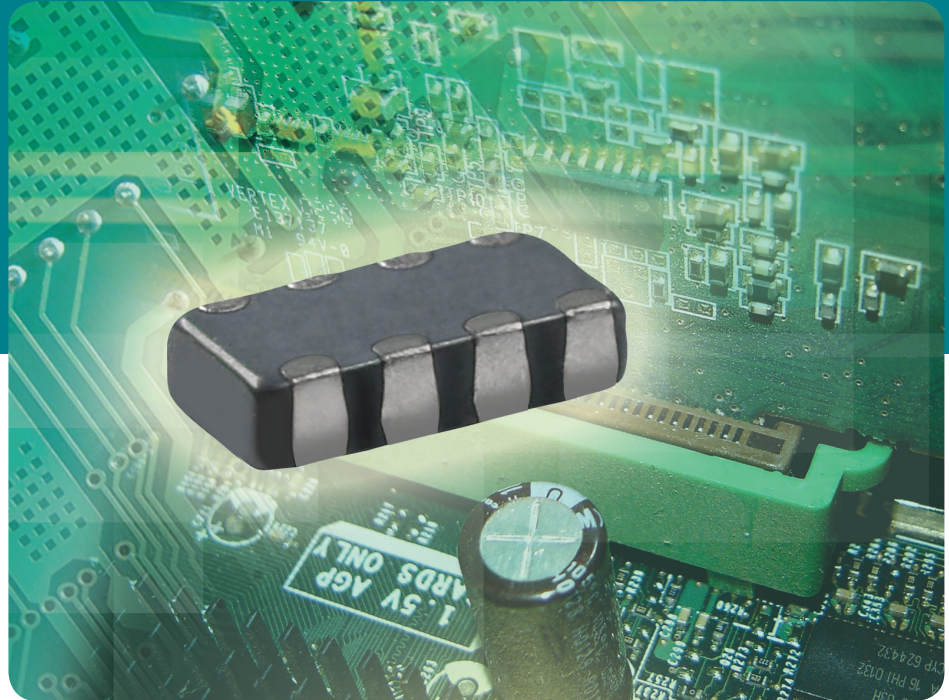




# SURFACE-MOUNT MULTILAYER CERAMIC CAPACITORS ARRAY

VJ...W1BC MLCC Chip Array



## Surface-Mount MLCC Array for Commodity Applications

### KEY BENEFITS

- Enables tighter, more compact circuit board layouts, which reduces board assembly costs
- Increases throughput
- Mounting cost saving
- Dry sheet manufacturing technology

### APPLICATIONS

- Controlling noise in digital and analog signal lines
- Computer motherboards and peripherals
- Common electronic circuits

## Surface-Mount Multilayer Ceramic Capacitors Array for Commodity Applications

### FEATURES

- High density mounting due to mounting space saving
- Mounting cost saving
- Increased throughput
- Dry sheet manufacturing technology
- Noble Metal Electrode system (NME) for COG (NPO)
- Base Metal Electrode system (BME) for X7R, Y5V
- Compliant to RoHS directive 2002/95/EC
- Halogen-free according to IEC 61249-2-21 definition

### APPLICATIONS

- For use as a bypass for digital and analog signal line noise
- Computer motherboards and peripherals
- The common electronic circuits



RoHS COMPLIANT HALOGEN FREE

ELECTRICAL SPECIFICATION	
Size	4 x 0603
Dielectric	COG (NPO) X7R Y5V
Capacitance (1)	10 pF to 470 pF 180 pF to 100 nF 10 nF to 100 nF
Capacitance Tolerance (2)	J ( $\pm 5\%$ ), K ( $\pm 10\%$ ) K ( $\pm 10\%$ ), M ( $\pm 20\%$ ) Z ( $-20\%$ to $+80\%$ )
Rated Voltage (Vdc)	50 V 16 V, 50 V 50 V
tan $\delta$ (1)	Cap. < 30 pF: Q $\geq 400 + 20$ C Cap. $\geq 30$ pF: Q $\geq 1000$ U <sub>R</sub> = 50 V, $\leq 2.5\%$ U <sub>R</sub> = 16 V, $\leq 3.5\%$
Insulation Resistance at U <sub>R</sub>	$\geq 10$ G $\Omega$ $\geq 10$ G $\Omega$ or R $\times$ C $\geq 500$ $\Omega$ $\times$ F, whichever is less
Operating Temperature	-55 °C to +125 °C -25 °C to +85 °C
Capacitance Change	$\pm 30$ ppm $\pm 15\%$
Termination	Ni/Sh lead (Pb)-free termination

### Notes

- (1) Measured at 30 % - 70 % related humidity  
NPO: apply 1.0 V<sub>RMS</sub>  $\pm 0.2$  V<sub>RMS</sub>, 1.0 MHz  $\pm 10\%$  at the conditions of 25 °C ambient temperature  
X7R: apply 1.0 V<sub>RMS</sub>  $\pm 0.2$  V<sub>RMS</sub>, 1.0 kHz  $\pm 10\%$  at the conditions of 25 °C ambient temperature  
Y5V: apply 1.0 V<sub>RMS</sub>  $\pm 0.2$  V<sub>RMS</sub>, 1.0 kHz  $\pm 10\%$  at the conditions of 20 °C ambient temperature
- (2) Preconditioning for X7R, Y5V, MLCC: Perform a heat treatment at 150 °C  $\pm 10$  °C for 1 h, then leave in ambient condition for 24 h  $\pm 2$  h before measurement.

ORDERING INFORMATION							
VJ06C4	100						
A	W1BC						
SIZE CODE	DIELECTRIC	CAPACITANCE	TOLERANCE	TERMINATION	RATED VOLTAGE	PACKAGING	PROCESS CODE FOR BASIC COMMODITY
06C4	A = COG (NPO) Y = X7R G = Y5V	Two significant digits followed by the number of zeros. R is in place of decimal point: 100 = 10 pF 101 = 100 pF	J = $\pm 5\%$ K = $\pm 10\%$ M = $\pm 20\%$ Z = $-20\%$ to $+80\%$	X = Ni Barrier	J = 16 V A = 50 V	C = 7" reel/paper tape	

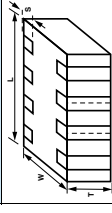
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For technical questions, contact [mlcc@vishay.com](mailto:mlcc@vishay.com)

SELECTION CHART			
DIELECTRIC	COG (NPO)	X7R	Y5V
STYLE	VJ06C4		
EIA CODE	0612 (4 x 0603)		
VOLTAGE V <sub>dc</sub>	50 V	16 V	50 V
VOLTAGE CODE	A	J	A
CAP. CODE	CAP.		
100	10 pF	B	A
150	15 pF	B	A
220	22 pF	B	A
330	33 pF	B	A
470	47 pF	B	A
680	68 pF	B	A
101	100 pF	B	A
151	150 pF	B	A
181	180 pF	B	A
221	220 pF	B	A
271	270 pF	B	A
331	330 pF	B	A
471	470 pF	B	A
102	1.0 nF	B	A
152	1.5 nF	B	A
222	2.2 nF	B	A
332	3.3 nF	B	A
472	4.7 nF	B	A
682	6.8 nF	B	A
103	10 nF	B	A
153	15 nF	B	A
223	22 nF	B	A
333	33 nF	B	A
473	47 nF	B	A
683	68 nF	B	A
104	100 nF	B	A

**Note**  
• Letters indicate product thickness, see packaging quantities

DIMENSIONS in inches [millimeters]						
SIZE	L	W	T MAX.	S	BW	P
0612 (1652)	0.125 $\pm$ 0.006 [3.20 $\pm$ 0.15]	0.063 $\pm$ 0.006 [1.60 $\pm$ 0.15]	0.036 [0.90]	0.012 $\pm$ 0.008 [0.30 $\pm$ 0.20]	0.016 $\pm$ 0.006 [0.40 $\pm$ 0.15]	0.031 $\pm$ 0.006 [0.80 $\pm$ 0.15]



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